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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,927	03/29/2001	Yusuke Tsutsui	81784.0232	7549

26021 7590 02/21/2003

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EXAMINER	
JORGENSEN, LELAND R	
ART UNIT	PAPER NUMBER
2675	6

DATE MAILED: 02/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,927	TSUTSUI ET AL.	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 6 and 13 are objected to because of the following informalities: Both describe "the oscillation circuit." There is insufficient antecedent basis for this limitation in the claims. The claim should read "an oscillation circuit." Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 3, 9, 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2 and 9 recites the limitation "the input voltage" in 19. There is insufficient antecedent basis for this limitation in the claim. Also, the claim describes no relationship between the input voltage and the supply voltage. Is the supply voltage the voltage produced after the input voltage is boosted or is it something else? Claims 3 and 10 are rejected as dependant on either rejected claim 2 or 9.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by West et al., USPN 5,537,650.

Claims 1 and 15

West describes a driving apparatus for a display device. The driving apparatus has a driving circuit for generating a signal to allow a display section to display. The driving circuit has a digital signal processing circuit for processing a digital signal, a digital-to-analog converter circuit for converting a digital signal to an analog signal, and an analog signal processing circuit for processing an analog signal. Although West does not specifically show a power supply circuit for generating a supply voltage for the driving circuit, West teaches that the power is decreased and increase. Thus, it is inherent that West have a power supply circuit. The power supply circuit reduces the supply voltage supplied to the digital-to-analog converter circuit and to the analog signal processing circuit, from the supply voltage during the normal operation, when specified power save operation are received. West, col. 2, lines 5 – 23; col. 3, lines 40 – 48; col. 4, lines 23 – 39; col. 4, line 6 – col. 5., line 1; col. 6, lines 19 – 23; col. 7, lines 29 – 41; and col. 8, lines 14 – 18.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over West in view of Iwamoto et al., USPN 4,544,912.

Claim 8

Iwamoto teaches an digital-to-analog converter circuit that includes a plurality of voltage dividing resistive elements connected in series to the power supply from the power supply circuit, divides the supply voltage into a plurality of stages by the voltage dividing resistive elements, selects a divided voltage corresponding to the digital data, and outputs an analog signal. Imamoto, col. 1, lines 11 – 16; col. 3, lines 3 – 26; and figure 3.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the digital-to-analog converter as taught by Iwamoto with the driving apparatus as taught by West. Iwamoto invites such combination by teaching,

> The present invention relates to a digital-to-analog converter (D/A converter). The D/A converter according to the present invention is used in, for example, an analog-to-digital conversion device of a step-by-step comparison type for processing signals in electronic circuit devices.

Iwamoto, col. 1, lines 11 – 16. Iwamoto discusses the disadvantages of prior art D/A converters. Of a first prior art D/A converter, Iwamoto teaches,

> However, such a prior art device is disadvantageous because another D/A converter must be provided to produce a variable reference voltage signal V_{ref} which is supplied to the D/A converter of FIG. 1 in order to effect analog control of the full-scale value V_f, and hence this prior art D/A converter device is very complicated.

Iwamoto, col. 2, lines 8 – 11. Of a second D/A converter, Iwamoto teaches,

> However, this prior art device is disadvantageous since it is difficult to carry out the automatic switching between the feedback resistors R_0 and R_0'

> using a digital signal, because it is necessary to change the connection of the connecting conductor W which connects the output of the AMP to one of the feedback resistors R_0 and R_0'. This method of controlling the full-scale value of the D/A converter of FIG. 2 is time-consuming and inconvenient.

Iwamoto, col. 2, lines 50 – 58. Iwamoto concludes,

> An object of the present invention is to eliminate the above described disadvantages in prior art D/A converters of the resistor network type.

Iwamoto, col. 3, lines 3 – 5.

8. Claims 2, 3, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over West or over West in view of Iwamoto as applied to claim 8 above, and further in view of Yatabe, USPN 6,297,622 B1.

Claims 2 and 9

Claim 2 and claim 9 each add details of the power supply circuit.

Neither West nor Iwamoto teach the details of the power supply circuit.

Yatabe teaches the details of the power supply circuit. Specifically, Yatabe teaches a power supply circuit that comprises a boosting section [control circuit 426, inductor coil 414, and diode 416]for boosting the input voltage [Vin] and a feedback section [resistors 420 and 422, and comparator 424] for detecting the supply voltage [Vout] at the output end of the power supply as a resistor divided voltage, comparing the detected voltage with a reference voltage [Vref], and controlling the boosting section so that the supply voltage is constant. Yatabe, col. 1, lines 12 – 28; and figure 3. Compare figure 4 and page 15, lines 14 – 21 of the specifications.

Yatabe teaches a plurality of resistive elements [resistors 420 and 422] connected to the output end of the power supply for detecting the supply voltage. A selector switch [switches

462, 464, and 466] for selecting a resistive element are connected to the feedback section from among the plurality of resistive elements. The divided voltage value of the supply voltage input to the feedback section is adjusted in response to the resistance value of the resistive element selected by the selector switch, and the output supply voltage is changed. Yatabe, col. 6, line 45 – col. 7, line 28.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit as taught by Yatabe with the driving apparatus as taught by West or West in view of Iwamoto. Yatabe invites such combination by teaching,

> The present invention relates to a power supply circuit for feeding power with a small loss, and an electro-optical device to which power is fed using the power supply circuit and which is characterized by low power consumption.

Yatabe, col. 1, lines 6 – 9. Yatabe adds,

> An object of the present invention is to at least provide a power supply circuit capable of minimizing power consumption and contributing to a compact and simple design, and to also provide an electro-optical device using the power supply circuit.

Yatabe, col. 2, lines 56 – 62. Yatabe specifically applies its design to a liquid crystal display device. Yatabe, col. 8, lines 43 – 56; and figure 8. Yatabe concludes,

> As described so far, according to the present invention, a current does not always flow through resistive elements. A loss in power caused by the resistive element scanning therefore be suppressed. Moreover, the resistive elements need not exhibit a high resistance. This contributes to a compact and simple design. Moreover, a power supply circuit becomes unsusceptible to noises.

Yatabe, col. 10, lines 58 – 64.

Claims 3 and 10

Yatabe teaches that a resistive element with a lower resistance value is selected by the selector switch when reduction in the output supply voltage is desired so that the divided voltage value input to the feedback section is increased. Yatabe, col. 6, line 45 – col. 7, line 28.

9. Claims 4, 5, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over West or over West in view of Iwamoto as applied to claim 8 above, and further in view of Nakanishi, USPN 6,323,851 B1.

Claims 4 and 11

Claims 4 and 11 each add details to the power supply circuit.

Neither West nor Iwamoto teach these details.

Nakanishi teaches a power supply circuit [power source circuit 21] that comprises a boosting section [booster circuit 210] for boosting the input voltage, a boosted power supply output switch [switch controller 213] for controlling passage between the boosting section and the output end of power supply, and a non-boosted power supply output switch [SW9] for bypassing the input and the output ends of power supply. Nakanishi, col. 4, line 34 – col. 5, line 48; col. 6, lines 12 – 59; col. 10, lines 49 – 57; and figure 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit as taught by Nakanishi with the driving apparatus as taught by West or West in view of Iwamoto so that the two types of output switches are switched and controlled such that one of the boosted or non-boosted supply voltages is output to the

digital-to-analog converter circuit and to the analog signal processing circuit. Nakanishi invites such combination by teaching,

> The present invention relates to a circuit and a method for driving a display device, more particularly to a circuit and a method for driving a display device which can prevent undesired bright lines or spots from appearing on a display screen when power supply is cut off.

Nakanishi, col. 1, lines 6 – 10. Nakanishi adds,

> A display device is driven with a voltage which is higher than a source voltage supplied from a battery or the like. To obtain such a drive voltage, a drive circuit of the display device comprises a booster circuit for boosting a source voltage from a battery or the like up to a plurality of predetermined high voltages. The drive circuit has its power source circuit and it outputs a plurality of different voltages because the display device needs different voltages to its scanning electrodes and signal electrodes for time-sharing addressing.
>
> A booster circuit or a dividing circuit is used as such a power source circuit which outputs a plurality of different voltages. The booster circuit boosts a source voltage into a plurality of different voltages. The booster circuit boosts a voltage by switching connection of a plurality of capacitors so that charged voltages in the capacitors are added to each other. The dividing circuit divides a previously boosted voltage into a plurality of different voltages. The dividing circuit divides a boosted source voltage with a series circuit of resistors or capacitors.
>
> A capacitor-based booster or dividing circuit is advantageous to reduce its power consumption.

Nakanishi, col. 1, lines 13 – 34. Nakanishi teaches the following objects and advantageous.

> The present invention has been made in consideration of the above, and it is an object to prevent irregular display caused by power-off action of the device from occurring.
>
> It is another object of the present invention to terminate activity of the display device without irregular display after the device is turned off.

Nakanishi, col. 1, lines 53 – 58. Nakanishi further adds,

> In the above embodiments, the following steps are taken. Discharging the capacitors, terminating the boost operation to reduce the boosted voltages and to

> terminate the output of the boosted voltages, and selecting a non-boosted voltage as a voltage to be applied. Those steps are performed in order to prevent irregular display during the off-state period from occurring and terminate display operation without occurrence of the irregular display.

Nakanishi, col. 10, lines 49 – 57. Nakanishi concludes with a description of its application to various types of displays.

> The driving circuit of the present invention may be used for not only the LCD device but for a PDP (plasma display panel), an EL (electroluminescent) display, an FED (field emission display), or the like. In other words, the driving circuit of the present invention may be used for a display device in which capacitors generate drive voltages and charges in the capacitors may cause irregular display during the off-state period.
>
> As described in the above, the present invention prevents irregular display from appearing on a display screen during an off-state period, thus, the display operation is terminated without occurrence of the irregular display.

Nakanishi, col. 13, lines 44 – 41.

Claims 5 and 12

Nakanishi teaches a power supply circuit [power source circuit 21] that comprises a boosting section [booster circuit 210] for boosting the input voltage, a boosted power supply output switch [switch controller 213] for controlling passage between the boosting section and the output end of power supply, and a non-boosted power supply output switch [SW9] for bypassing the input and the output ends of power supply. Nakanishi, col. 4, line 34 – col. 5, line 48; col. 6, lines 12 – 59; col. 10, lines 49 – 57; and figure 2. The boosting section [booster circuit 210] includes a plurality of capacitors [boosting capacitors C-1 to C-4] and a plurality of switches [SW1 to SW8] for the capacitors, for boosting an input voltage by switching and controlling the plurality of switches for capacitors. Nakanishi, col. 4, line 34 – 57; and figure 2. A clock signal produced by the driving circuit is used for switching and controlling the plurality

of switches for capacitors. Nakanishi, col. 12, lines 49 – 62. It is inherent that the clock signal is produced by a clock.

For the reasons stated in the discussion about claims 4 and 13, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit as taught by Nakanishi with the driving apparatus as taught by West or West in view of Iwamoto.

10. Claims 6, 7, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over West in view of Nakanishi as applied to claim 5 above or over West in view of Iwamoto and further in view of Nakanishi as applied to claim 12 above, and further in view of Niijima, USPN 5,155,840.

Claims 6 and 13

West and Nakanishi teach that the driving circuit determines a current mode from a boosted power supply generating mode, a non-boosted power supply generating mode, or a power supply suspension mode, based on a predetermined power save control instruction, and based on the determination controls supply and suspension of supply of the power supply clock or supply and suspension of supply of the clock, and opening/closing of the output switches of the power supply circuit.

Neither West, Nakanishi, nor Iwamoto teach that the clock signal is from an oscillation circuit.

Niijima teaches clock to generate signals from a oscillation circuit [Sub System-Clock Oscillation Circuit 4 and Main System-Clock Oscillation Circuit 5]. Niijima, col. 5, lines 22 – 40; and figure 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention have to combine the clock having an oscillation circuit with the driving apparatus as taught by West and Nakanishi or West, Nakanishi, or Iwamoto. Niijima invites such combination by teaching,

> The present invention relates to a single-chip microcomputer which possesses internally a clock-signal switching function and, more particularly, to a single-chip microcomputer capable of automatically stopping the oscillation of a main system-clock oscillation circuit after a clock signal has been switched to a sub clock-signal from a main clock-signal.
>
> Today, one of the capabilities which is sought in a single-chip microcomputer is that of reducing power consumption.
>
> A conventional example in which an attempt has been made to reduce power consumption is one which employs two oscillators, one being a main system-clock oscillator for a high speed operation and the other being a sub system-clock oscillator for a low speed operation.
>
> In this conventional example, during the period in which the single-chip microcomputer is operable by the clock-signal for a low speed operation, the main system-clock oscillation circuit stops its operation and only the sub system-clock oscillation circuit which is slow in speed but in which the power consumption is small operates. Such a conventional single-chip microcomputer and a problem therein are fully explained later for assisting the understanding of the present invention.

Niijima, col. 1, lines 8 – 32. Niijima teaches as an object of the invention,

> It is, therefore, an object of the present invention to overcome the problem existing in the conventional arrangement and to provide an improved single-chip microcomputer.
>
> It is another object of the present invention to provide a single-chip microcomputer which is capable of effecting an automatic stop of a main system-

> clock oscillation circuit after a main clock-signal has been switched to a sub clock-signal.

Niijima, col. 1, lines 35 - 44.

Claims 7 and 14

Nakanishi teaches a power supply circuit [power source circuit 21] that comprises a boosting section [booster circuit 210] for boosting the input voltage, a boosted power supply output switch [switch controller 213] for controlling passage between the boosting section and the output end of power supply, and a non-boosted power supply output switch [SW9] for bypassing the input and the output ends of power supply. Nakanishi, col. 4, line 34 – col. 5, line 48; col. 6, lines 12 – 59; col. 10, lines 49 – 57; and figure 2. The boosting section [booster circuit 210] includes a plurality of capacitors [boosting capacitors C-1 to C-4] and a plurality of switches [SW1 to SW8] for the capacitors, for boosting an input voltage by switching and controlling the plurality of switches for capacitors. Nakanishi, col. 4, line 34 – 57; and figure 2. A clock signal produced by the driving circuit is used for switching and controlling the plurality of switches for capacitors. Nakanishi, col. 12, lines 49 – 62. It is inherent that the clock signal is produced by a clock.

For the reasons stated in the discussion about claims 4 and 13, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit as taught by Nakanishi with the driving apparatus as taught by West or West in view of Iwamoto.

Niijima teaches clock to generate signals from a oscillation circuit [Sub System-Clock Oscillation Circuit 4 and Main System-Clock Oscillation Circuit 5]. Niijima, col. 5, lines 22 – 40; and figure 1.

For the reasons stated above in the discussion about claims 6 and 13, it would have been obvious to one of ordinary skill in the art at the time of the invention have to combine the clock having an oscillation circuit with the driving apparatus as taught by West and Nakanishi or West, Nakanishi, or Iwamoto.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Davis et al., USPN 4,355,277, teaches a duel mode DC/DC converter.

Miller et al., USPN 4,155,112, teaches a power supply circuit.

Schwob, USPN 4,584,517, teaches a DC/DC voltage regulator.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

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or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

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